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EXAMINER	
YIGDALL, MICHAEL J	

ART UNIT	PAPER NUMBER
2192	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/802,857	KOH ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114 was filed in this application after a decision by the Board of Patent Appeals and Interferences, but before the filing of a Notice of Appeal to the Court of Appeals for the Federal Circuit or the commencement of a civil action. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114.

Applicant's submission filed on August 21, 2007 has been entered. Claims 26-44 are now pending.

Response to Amendment

2. The rejection of claims 13-25 under 35 U.S.C. 103(a) has been withdrawn in view of Applicant's amendment canceling those claims.

Response to Arguments

3. Applicant's arguments with respect to new claims 26-44 have been considered but are moot in view of the new ground(s) of rejection, as set forth below.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 31 and 37-39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicant regards as the invention.

With respect to claim 31 (new), the claim recites, "said random access memory," for which there is insufficient antecedent basis in the claims. The examiner's interpretation is that the data processing apparatus as set forth in claim 30 comprises random access memory.

With respect to claim 37 (new), the claim recites, "said another buggy part," for which there is insufficient antecedent basis in the claims. The examiner's interpretation is as if claim 37 were dependent upon claim 35.

With respect to claim 38 (new), the claim recites, "said another bug address," for which there is insufficient antecedent basis in the claims. The examiner's interpretation is as if claim 38 were dependent upon claim 35.

With respect to claim 39 (new), the claim recites, "said random access memory," for which there is insufficient antecedent basis in the claims. The examiner's interpretation is that the data processing apparatus as set forth in claim 34 comprises random access memory.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 26-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,454,100 to Sagane (art of record, "Sagane") in view of U.S. Patent No. 5,784,537 to Suzuki et al. (now made of record, "Suzuki").

With respect to claim 26 (new), Sagane teaches a data processing apparatus (see, for example, electronic apparatus 1 in FIG. 1) comprising:

program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes (see, for example, ROM 3 in FIG. 1 and column 1, lines 9-14, which shows that the ROM is program memory that stores instruction codes as a program, and column 3, lines 48-52, which shows that an execution or program address indicates a location in the ROM);

a bug address setting register adapted to store a bug address, said bug address indicating a starting address within said program memory for a buggy part of said program (see, for example, interrupt generating address register 9 in FIG. 1 and column 3, lines 40-43, which shows that the register stores a correction or bug address, and column 3, lines 32-39, which shows that the correction address indicates a starting address within the ROM of a buggy part of the program).

Sagane further teaches an interrupt request signal that indicates a coincidence between said program address and said bug address (see, for example, column 3, lines 59-61, which shows an interrupt request signal, and column 3, lines 48-52, which shows that the interrupt request signal indicates a coincidence between the execution address and the correction address), but does not expressly disclose:

a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address.

Nonetheless, Sagane teaches that the interrupt request signal is generated a number of times (see, for example, steps S7 and S8 in FIG. 2). Sagane further teaches that if the ROM includes a plurality of buggy parts, then the interrupt generating address register is updated each time to reflect the next correction address (see, for example, column 5, lines 49-54). Thus, it is necessary for Sagane to track which correction address is the next correction address. To do so, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to track the number of times the interrupt request signal is generated, such as with a value stored in a register.

For example, in an analogous art, Suzuki teaches a PC comparison register section 20 that generates a ROM correction interruption request to a CPU 14 to indicate coincidence between the program address and a correction execution interruption address (see, for example, FIG. 1 and column 6, lines 27-35). Suzuki further teaches storing a value that represents the number of correcting portions (i.e., the number of buggy parts) and decrementing the value each time coincidence is indicated (see, for example, step S5 in FIG. 4A and step S28 in FIG. 4B). Thus, the value also represents the number of times coincidence is indicated.

Therefore, as Suzuki further suggests, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate within the data processing apparatus of Sagane, a counter register adapted to store a value, said value

representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address.

With respect to claim 27 (new), the rejection of claim 26 is incorporated, and Sagane in view of Suzuki further teaches:

a coincidence detecting circuit adapted to compare said program address with said bug address and output said interrupt request signal (see, for example, comparator 8 in FIG. 1 and column 3, lines 48-52, which shows that the comparator compares the execution address with the correction address and outputs a coincidence signal, and column 3, lines 59-61, which shows that the coincidence signal is output as the interrupt request signal),

wherein said interrupt request signal indicates coincidence or non-coincidence of said program address and said bug address (see, for example, column 5, lines 11-16, which shows that the interrupt request signal indicates coincidence or non-coincidence of the addresses).

With respect to claim 28 (new), the rejection of claim 27 is incorporated, and Sagane in view of Suzuki further teaches that said value is incremented when said interrupt request signal indicates said coincidence (see, for example, Suzuki, step S28 in FIG. 4B, which shows that the value is decremented when coincidence is indicated).

A person having ordinary skill in the art at the time the invention was made could implement the counter register such that the value is incremented rather than decremented with predictable results. To do so, for example, one could implement Suzuki such that the value is initialized to 0 and step S29 (FIG. 4B) checks for whether the value is equal to the number stored in step S5 (FIG. 4A), rather than checking for whether the value is equal to 0.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane and Suzuki such that said value is incremented when said interrupt request signal indicates said coincidence.

With respect to claim 29 (new), the rejection of claim 26 is incorporated, and Sagane in view of Suzuki further teaches:

a central processing unit adapted to receive said interrupt request signal (see, for example, CPU 2 in FIG. 1).

With respect to claim 30 (new), the rejection of claim 29 is incorporated, and Sagane in view of Suzuki further teaches that said central processing unit reads an abort vector from said program memory when said interrupt request signal indicates said coincidence (see, for example, column 5, lines 16-21, which shows that the CPU reads an abort vector when the interrupt request signal indicates coincidence),

said abort vector indicating a starting address for a debugged program (see, for example, column 5, lines 16-21, which shows that the abort vector indicates a starting address for a correction or debugged program).

With respect to claim 31 (new), the rejection of claim 30 is incorporated, and Sagane in view of Suzuki further teaches that said abort vector is located within said random access memory (see, for example, column 5, lines 44-48, which shows that the abort vector is located within RAM).

With respect to claim 32 (new), the rejection of claim 29 is incorporated, and Sagane in view of Suzuki further teaches that said central processing unit receives said interrupt request signal (see, for example, FIG. 1, which shows that the CPU receives the interrupt request signal via interrupt control circuit 7d).

With respect to claim 33 (new), the rejection of claim 29 is incorporated, and Sagane in view of Suzuki further teaches that said central processing unit reads said instruction codes sequentially from said program memory (see, for example, column 5, lines 28-31, which shows that the CPU reads instruction codes sequentially from the ROM).

With respect to claim 34 (new), the rejection of claim 29 is incorporated, and Sagane in view of Suzuki further teaches that another program address indicates a location within said program memory for another of the instruction codes (see, for example, column 3, lines 48-52, which shows that another execution or program address indicates another location in the ROM).

With respect to claim 35 (new), the rejection of claim 34 is incorporated, and Sagane in view of Suzuki further teaches:

another bug address setting register adapted to store another bug address, said another bug address indicating another starting address within said program memory for another buggy part of said program (see, for example, interrupt generating address register 9 in FIG. 1 and column 3, lines 40-43, which shows that the register stores a correction or bug address, and column 3, lines 32-39, which shows that the correction address indicates a starting address within the ROM of a buggy part of the program).

As noted above, Sagane teaches that if the ROM includes a plurality of buggy parts, then the interrupt generating address register is updated each time to reflect the next correction address (see, for example, column 5, lines 49-54). In an analogous embodiment, Sagane similarly teaches a correction address register that is updated to reflect the next correction address (see, for example, column 6, lines 63-67), and further suggests, as an alternative, providing a plurality of correction address registers for the plurality of buggy parts (see, for example, column 6, line 67 to column 7, line 3). A person having ordinary skill in the art at the time the invention was made could incorporate a plurality of interrupt generating address registers into the data processing apparatus of Sagane with predictable results.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane and Suzuki so as to comprise another bug address setting register adapted to store another bug address, said another bug address indicating another starting address within said program memory for another buggy part of said program.

With respect to claim 36 (new), the rejection of claim 35 is incorporated, and Sagane in view of Suzuki further teaches that said value is incremented when another interrupt request signal indicates another coincidence between said program address and said another bug address (see, for example, Suzuki, step S28 in FIG. 4B, which shows that the value is decremented when coincidence is indicated).

A person having ordinary skill in the art at the time the invention was made could implement the counter register such that the value is incremented rather than decremented with predictable results. To do so, for example, one could implement Suzuki such that the value is

initialized to 0 and step S29 (FIG. 4B) checks for whether the value is equal to the number stored in step S5 (FIG. 4A), rather than checking for whether the value is equal to 0.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane and Suzuki such that said value is incremented when another interrupt request signal indicates another coincidence between said program address and said another bug address.

With respect to claim 37 (new), the rejection of claim 35 is incorporated, and Sagane in view of Suzuki further teaches that said central processing unit is adapted use said value to select for correction said buggy part or said another buggy part (see, for example, Suzuki, column 6, line 65 to column 7, line 7, which shows that the value is used to select the corresponding buggy part for correction).

With respect to claim 38 (new), the rejection of claim 35 is incorporated, and Sagane in view of Suzuki further teaches:

another coincidence detecting circuit adapted to compare said another program address with said another bug address and output another interrupt request signal (see, for example, comparator 8 in FIG. 1 and column 3, lines 48-52, which shows that the comparator compares the execution address with the correction address and outputs a coincidence signal, and column 3, lines 59-61, which shows that the coincidence signal is output as the interrupt request signal),

wherein said another interrupt request signal indicates coincidence or non-coincidence of said another program address and said another bug address (see, for example, column 5, lines 11-

16, which shows that the interrupt request signal indicates coincidence or non-coincidence of the addresses).

As noted above, Sagane teaches that if the ROM includes a plurality of buggy parts, then the interrupt generating address register is updated each time to reflect the next correction address (see, for example, column 5, lines 49-54). In an analogous embodiment, Sagane similarly teaches a correction address register that is updated to reflect the next correction address (see, for example, column 6, lines 63-67), and further suggests, as an alternative, providing a plurality of correction address registers and a plurality of comparators for the plurality of buggy parts (see, for example, column 6, line 67 to column 7, line 3). A person having ordinary skill in the art at the time the invention was made could incorporate a plurality of comparators into the data processing apparatus of Sagane with predictable results.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane and Suzuki so as to comprise another coincidence detecting circuit adapted to compare said another program address with said another bug address and output another interrupt request signal, wherein said another interrupt request signal indicates coincidence or non-coincidence of said another program address and said another bug address.

With respect to claim 39 (new), the rejection of claim 34 is incorporated, and Sagane in view of Suzuki further teaches that said counter register is located within said random access memory at a predetermined memory address (see, for example, Suzuki, column 5, lines 41-46, which shows that the value is stored at a predetermined location in RAM).

With respect to claim 40 (new), the rejection of claim 34 is incorporated, and Sagane in view of Suzuki further teaches that said value of the counter register is incremented by 1 (see, for example, Suzuki, step S28 in FIG. 4B, which shows that the value is decremented by 1 when coincidence is indicated).

A person having ordinary skill in the art at the time the invention was made could implement the counter register such that the value is incremented by 1 rather than decremented by 1 with predictable results. To do so, for example, one could implement Suzuki such that the value is initialized to 0 and step S29 (FIG. 4B) checks for whether the value is equal to the number stored in step S5 (FIG. 4A), rather than checking for whether the value is equal to 0.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane and Suzuki such that said value of the counter register is incremented by 1.

With respect to claim 41 (new), the rejection of claim 34 is incorporated, and Sagane in view of Suzuki further teaches that debugged programs are stored within a random access memory (see, for example, RAM 4 in FIG. 1 and column 3, lines 43-44, which shows that correction or debugged programs are stored in the RAM).

With respect to claim 42 (new), the rejection of claim 41 is incorporated, and Sagane in view of Suzuki further teaches that said debugged programs stored within said random access memory is read from an external memory (see, for example, EEPROM 13 in FIG. 1 and column 3, lines 43-44, which shows that the correction programs are read from an external memory).

With respect to claim 43 (new), the rejection of claim 41 is incorporated, and Sagane in view of Suzuki further teaches that said debugged programs are stored within said random access memory during initialization processing (see, for example, column 3, lines 45-46, which shows that the correction programs are stored in RAM during initialization).

With respect to claim 44 (new), the rejection of claim 43 is incorporated, and Sagane in view of Suzuki further teaches that said counter register is cleared during said initialization processing (see, for example, Suzuki, column 5, lines 41-46, which shows that the value is stored in RAM, and column 4, lines 1-5, which shows that the value in RAM is cleared during initialization).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (571) 272-3707. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael J. Yigdall
Examiner
Art Unit 2192

mjy

Michael Yigdall